What is claimed is:

1. A processor, comprising:

an arithmetic unit for processing operands;

a register memory for storing operands; and

a register memory configuration unit designed to configure the register memory such that memory space in the register memory is assigned to operands and that memory space in the register memory that is not assigned to operands is made available for other data than the operands.

2. The processor according to claim 1, wherein the arithmetic unit, the register memory and a control unit for controlling the arithmetic unit and the register memory for loading operands from the register memory into the arithmetic unit and for carrying out an operation with the operands are designed as integrated circuit on a single chip.

3. The processor according to claim 1 , wherein the operands are long number operands comprising a length of more than 150 bits.

4. The processor according to claim 1, further comprising an external memory and an addressing unit, wherein the addressing is designed to address the remaining memory space of the register memory like the external memory.

5. The processor according to claim 1, wherein the arithmetic unit is designed to perform at least two algorithms, wherein one algorithm needs a maximum amount of register memory space due to its length and/or number of its used operands, while another

algorithm needs a smaller amount of register memory space for its operands,

wherein the register memory is dimensioned such that the register memory space it at least equal to the maximum amount of register memory space needed by an algorithm for its operation.

6. The processor according to claim 1, which is designed to carry out a cryptographic algorithm.

7. The processor according to claim 1, wherein the arithmetic unit and the register memory are connected via an internal bus,

wherein an external element is connected to the arithmetic unit via an external bus, and

wherein the length of the external bus is greater than the length of the internal bus.

8. The processor according to claim 1, wherein the register memory configuration unit is disposed to configure registers of different number and length in the register memory as needed.

9. A computer system, comprising:

a host CPU;

a peripheral device connected to the host CPU via an external bus comprising an internal memory; and

a memory configuration unit, the memory configuration unit being designed to make space from the internal memory available for the peripheral device as needed, and to make space from the internal memory not being made available to the peripheral device available for

other data by access via an external bus.

10. The computer system according to claim 9, further comprising an addressing means, wherein the addressing means is disposed to address the internal memory of the peripheral device, which is not made available to the peripheral device, like an external memory of the computer system.

11. The computer system according to claim 9, wherein the register memory configuration unit is part of the peripheral device.

12. The computer system according to claim 9, wherein the memory configuration unit is disposed to check whether the peripheral device is active and in the case when the peripheral device is not active, to make the whole internal memory of the peripheral device available for the computer system as working memory.

13. The computer system according to claim 9, wherein the peripheral device is a cryptocoprocessor.

14. The computer system according to claim 9, designed as chip card IC or security IC.